

North South University

Center of Excellence in Higher Education

CSE231.2

Term Project-SP18

Phase 3: Final Demonstration

Group : **7**

Group Members:

|  |  |
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Submitted to:

**Dr. Arshad M. Chowdhury**

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**Objectives:**

* Design a complete logic system from specification to implementation
* Coordination between the combinational and the sequential parts
* Become familiarized with the analysis of combinational logic networks and Synchronous Sequential Logic
* Learn the implementation of networks using Logic gates, decoders or MUX
* We need to display “**SP18-CSE231-7**” if the Direction input is logic **LOW** and the reverse order (“**7-132ESC-81PS**”) if the Direction input is logic **HIGH**

**List of Equipment:**

* Seven-Segment Display
* Voltage Regulator
* Voltage source1
* Breadboard
* Switch
* Wires

**Combinational Part:**

* IC 74151 (8:1 Multiplexers) - 7 piece
* IC 7404 (NOT Gates) - 1 piece

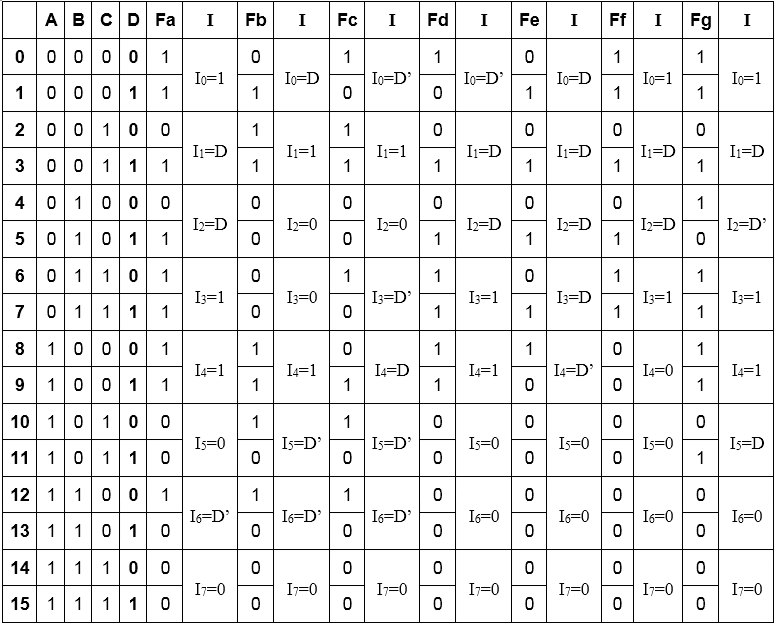
**Sequential Part:**

* IC 7473 (JK Flip-Flop) - 2 piece
* IC 7421 (4-input AND gate) - 1 piece
* IC 7411 (3-input AND gate) - 2 piece
* IC 7408 (2-input AND gate) - 2 piece
* IC 4072 (4-input OR gate) - 1 piece
* IC 4075 (3-input OR gate) - 1 piece
* IC 7432 (2-input OR gate) - 1 piece
* Timer IC 555 - 1 piece
* 10K Resistor - 1 piece
* 100uF Capacitor - 1 piece

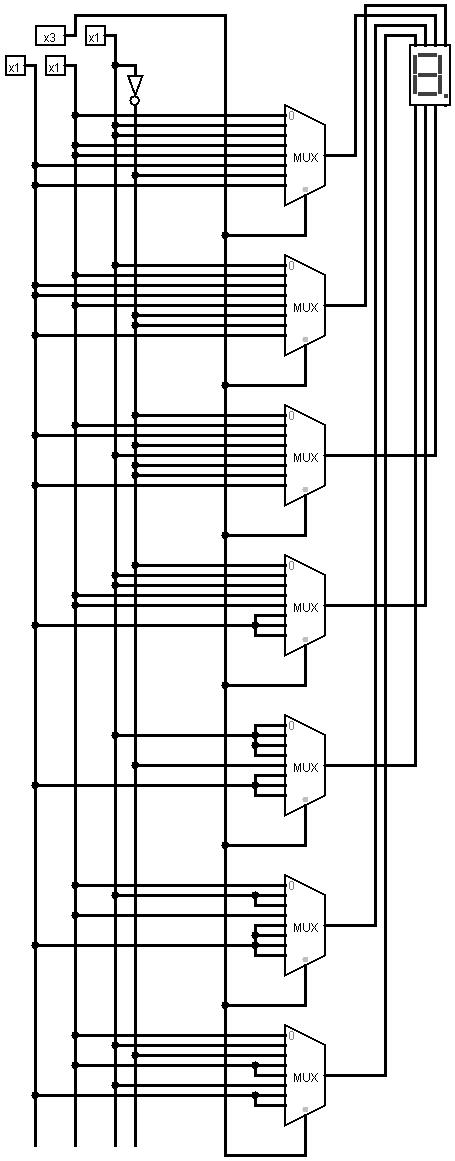
**Phase 1: Combinational Circuit Design and Implementation**

**(Using 8:1 MUX)**

**Truth Table:**

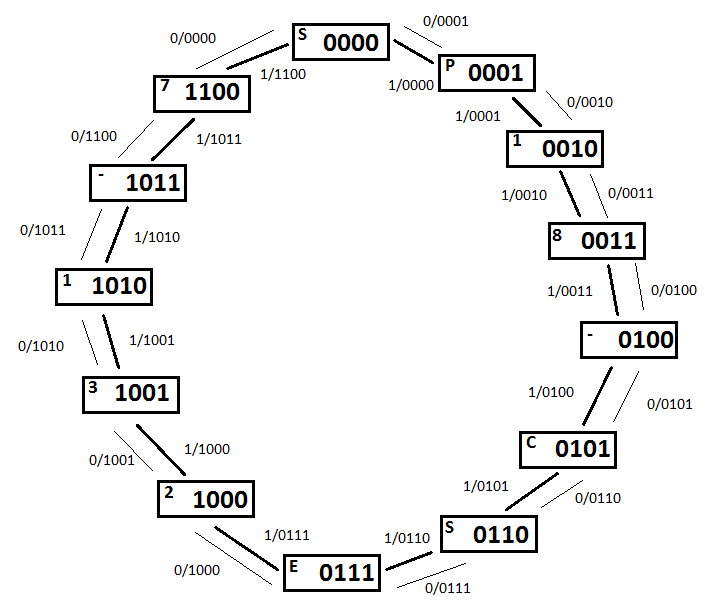
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**Block Diagram:**

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**Phase 2: Sequential Circuit design**

**State Diagram:**

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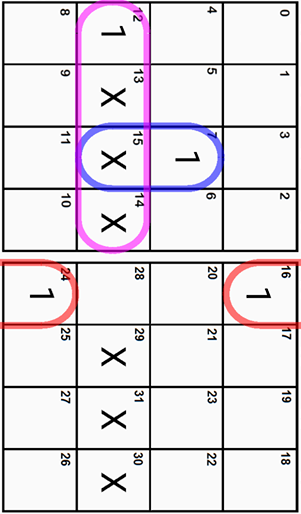
**State Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | **Present State** | | | | |  | **Next State** | | | | |  | **Flip Flop Inputs** | | | |
| **A** | **State** | **Bt** | **Ct** | **Dt** | **Et** | **State** | **Bt+1** | **Ct+1** | **Dt+1** | **Et+1** | **TB** | **TC** | **TD** | **TE** |
| 0 | S | 0 | 0 | 0 | 0 |  | P | 0 | 0 | 0 | 1 |  | 0 | 0 | 0 | 1 |
| 0 | P | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 8 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 8 | 0 | 0 | 1 | 1 | - | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | - | 0 | 1 | 0 | 0 | C | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | C | 0 | 1 | 0 | 1 | S | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | S | 0 | 1 | 1 | 0 | E | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | E | 0 | 1 | 1 | 1 | 2 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 2 | 1 | 0 | 0 | 0 | 3 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 3 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | - | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | - | 1 | 0 | 1 | 1 | 7 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 7 | 1 | 1 | 0 | 0 | S | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0 |  | 1 | 1 | 0 | 1 |  | X | X | X | X | X | X | X | X |
| 0 |  | 1 | 1 | 1 | 0 |  | X | X | X | X | X | X | X | X |
| 0 |  | 1 | 1 | 1 | 1 |  | X | X | X | X | X | X | X | X |

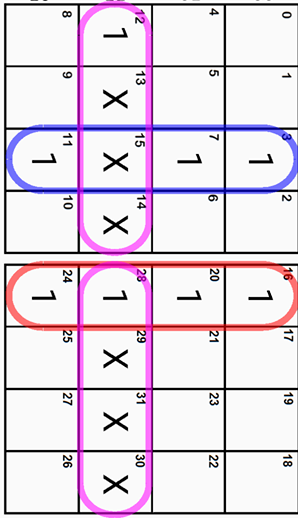
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input** | **Present State** | | | | |  | **Next State** | | | | |  | **Flip Flop Inputs** | | | |
| **A** | **State** | **Bt** | **Ct** | **Dt** | **Et** | **State** | **Bt+1** | **Ct+1** | **Dt+1** | **Et+1** | **TB** | **TC** | **TD** | **TE** |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | S | 0 | 0 | 0 | 0 |  | 7 | 1 | 1 | 0 | 0 |  | 1 | 1 | 0 | 0 |
| 1 | P | 0 | 0 | 0 | 1 | S | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | P | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 8 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | - | 0 | 1 | 0 | 0 | 8 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | C | 0 | 1 | 0 | 1 | - | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | S | 0 | 1 | 1 | 0 | C | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | E | 0 | 1 | 1 | 1 | S | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 2 | 1 | 0 | 0 | 0 | E | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 3 | 1 | 0 | 0 | 1 | 2 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 3 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | - | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 7 | 1 | 1 | 0 | 0 | - | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 |  | 1 | 1 | 0 | 1 |  | X | X | X | X | X | X | X | X |
| 1 |  | 1 | 1 | 1 | 0 |  | X | X | X | X | X | X | X | X |
| 1 |  | 1 | 1 | 1 | 1 |  | X | X | X | X | X | X | X | X |

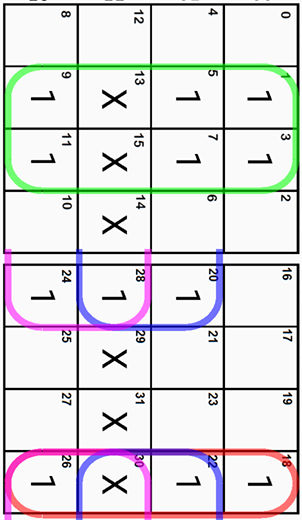
**Karnaugh map (K-map):**

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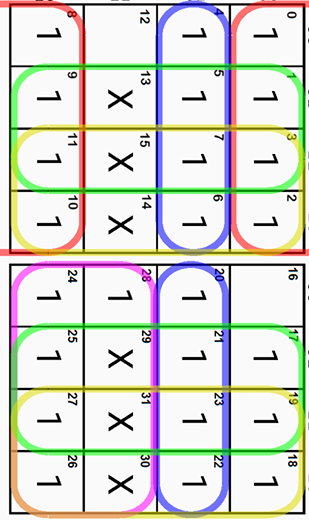
**TB = **

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**TC = **

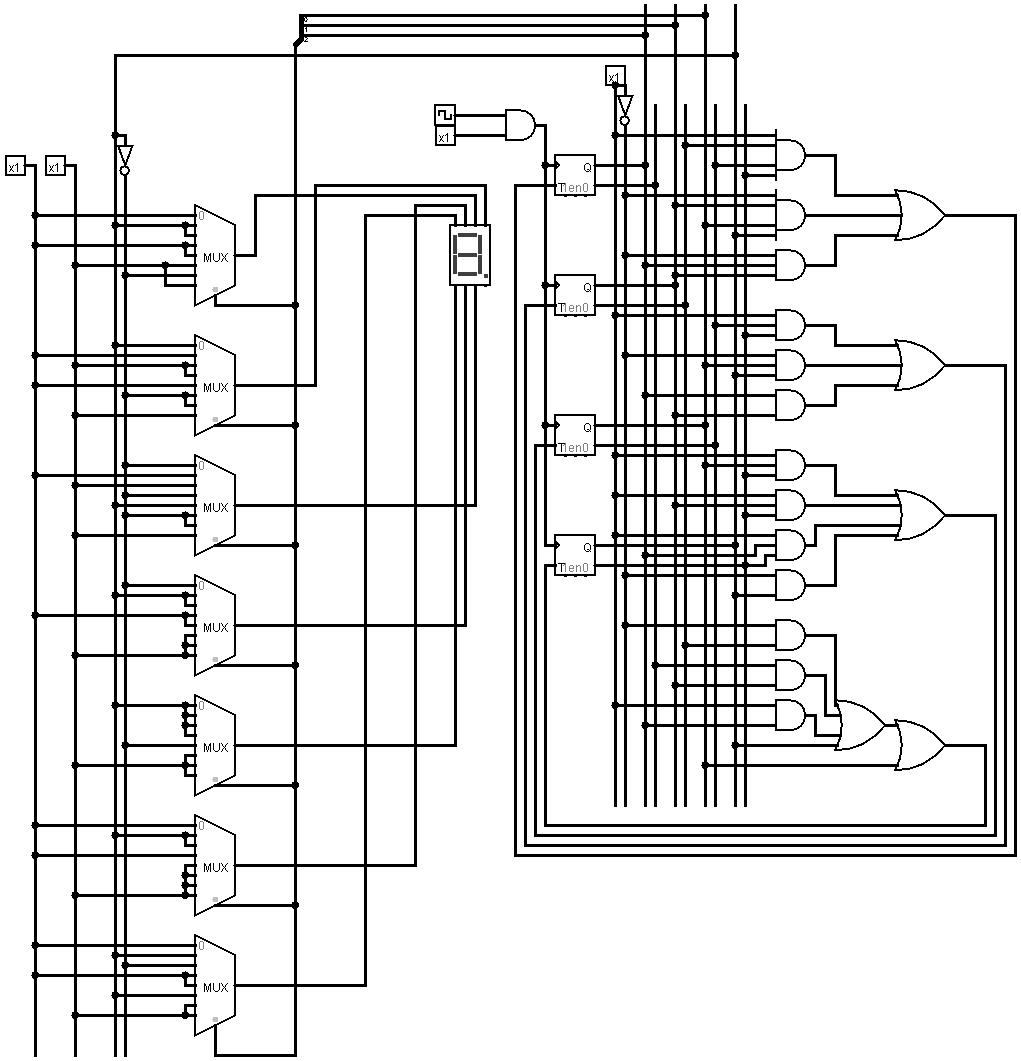
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**TD = **

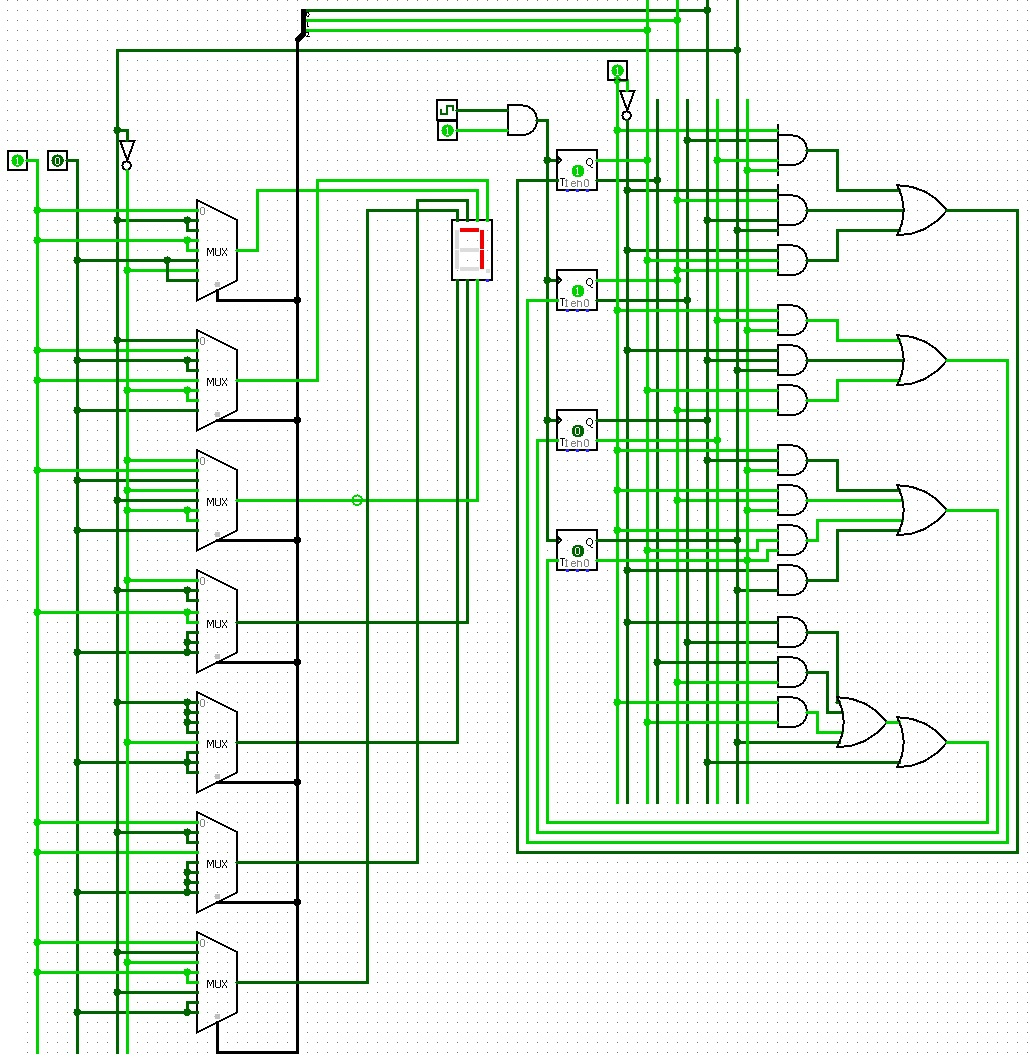
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**TE = **

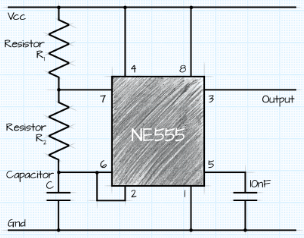
**Circuit Diagram :**

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**Simulation :**

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**Clock Circuit:**

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R = R =10k Ohm & C = 100uF

**Discussion**:

From the truth table it can be seen that, the number of input bits is four (A,B,C,D) and the number of output bits is seven (Fa,Fb,Fc,Fd,Fe,Ff,Fg). We have assigned the number (0-12) for the inputs. We have considered 0 (zero) for the last three inputs. Afterwards,we have constructed the truth table accordingly and with the help of the K-map we obtained minimal term for each of the seven output functions (Fa,Fb,Fc,Fd,Fe,Ff,Fg). Later, we have simulated the circuit with logisim with basic gates, 3:8 decoder and 8:1 multiplexer.

However, we have chosen to conduct the experiment using multiplexer.

Upon analysis of the state table, it was clear that **T** Flip Flops would give a simplified circuit. However, T FFs were not available in the market so we decided to make **T** Flip Flops using **JK** Flip Flop. Behind this decision we had to consider a few facts for instance

efficiency, complexity, cost consideration etc.

From the figure we found that for both **D** Flip Flop and **JK** the Literal cost (L), Gate input cost (G), Gate input cost including inverters (GN) are much higher than the **T** Flip Flops. Also it will be a very complicated circuit where relatively more wiring is required and also the cost of implementation is higher. Thus we have decided to use **T** Flip Flops to implement the circuit.